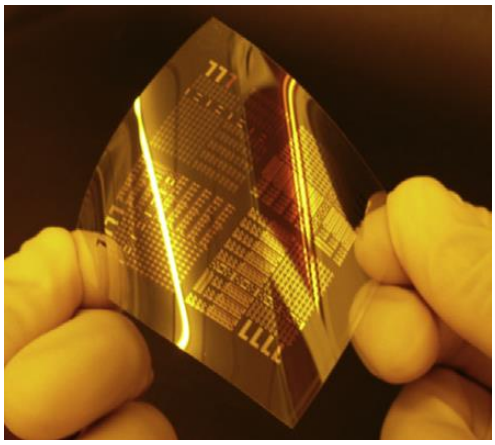
Master Thesis

Modeling of Organic Thin-Film Transistors for Electronic-Design-Automation Tools

Organic thin-film transistors (OTFTs) are field-effect transistors with a semiconducting organic channel. They are fabricated with low-temperature and low-cost processing and printing techniques, resulting in the possibility to integrate complex electronic circuits on flexible organic films. OTFT technologies have thus attracted the attention of scientific and industrial communities for its application in biomedical and analog signal-processing microelectronics.
In order to predict the static and dynamic performance of analog circuits, accurate modelling of such devices is needed. The growing complexity of circuit designs requires these models also to be adapted and embedded in state-of-the-art Electronics-Design-Automation (EDA) tools. In such design tools, the user instantiates so-called parametric cells (p-cells) of a component into larger schematics, e.g., a single transistor into an amplifier. These cells consist of a symbol with connection terminals, a unique model binding and assigned user-parameters, e.g., the width and length of the transistor. During circuit simulation, the user parameters are automatically fed to the behavioral model of the transistor. Furthermore, when placing a parametrized device into a layout view, the physical dimensions are automatically fitted to the values specified by the user.

The goal of this thesis is to investigate the size-scaling capability of different model parameters and the feasibility of an implementation as a transistor p-cell. The work will focus on the analysis of dominant parasitic properties in OTFTs, as for example the contact resistance. Furthermore, in order to enhance EDA layout tools, the possibility of a physical p-cell implementation should be addressed.

The thesis provides the opportunity to gain an in-depth understanding of present and novel OTFT technologies and allows gathering experience with state-of-the-art analog design flows, design tools, and behavioral modeling. A basic understanding of CMOS analog circuit design, basic transistor modeling, as well as an easy handling with new programming and scripting languages should be considered as prerequisite.



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