## Master Thesis

# Development of a Block-based Statistical Timing Model for Low-Voltage Combinatorial Logic

Today, digital circuits are pushed to the limits not only with respect to performance, but also power consumption and efficiency. Reducing the supply voltage of digital circuits is a widely used concept to reduce the power consumption of digital circuits. However, it poses several unique challenges at extremely low levels of the supply voltage. Due to the manufacturing process, one of these challenges is the increasing uncertainty in signal integrity and circuit delay as illustrated in Fig. 2.

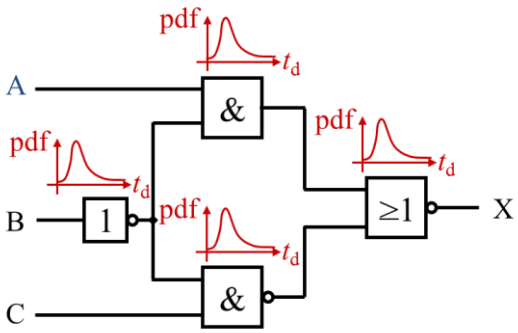


**Figure 1: Combinatorial block with variable delay**

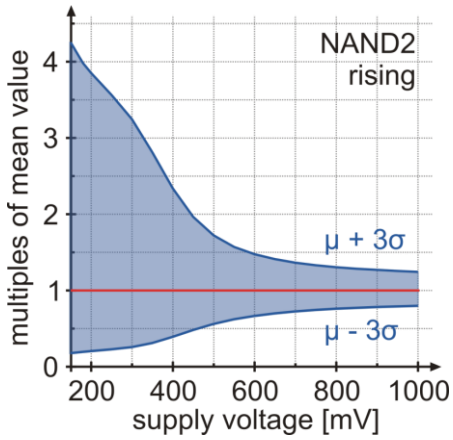


**Figure 2: Normalized 3σ values of gate delay at various supply voltages**

The research goal of this thesis is to expand a path-based statistical timing model to a block-based model. An algorithm is to be developed and implemented, which is capable to determine the statistical distribution of the timing behavior of a combinatorial logic block as illustrated in Fig 1. This has to be done based on characterization data of the constituent elements and a netlist describing the circuit topology.

**What we expect:**
Interests in electronic circuits and their modeling, willingness to familiarize with the topic and the simulation software, well documented work, and teamwork.

**What we offer:**
Intensive supervision of the thesis, nice work environment and teamwork, latest simulation software tools, data analysis tools and free space for own ideas.

**Starting Date:** As soon as possible

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