Master Thesis

Development of a Schmitt-Trigger Based Ultra-Low-Voltage SRAM

Today, digital circuits are pushed to the limits not only with respect to performance, but also power consumption and efficiency. Reducing the supply voltage of digital circuits is a widely used concept, which poses unique challenges especially with regard to memory cells.

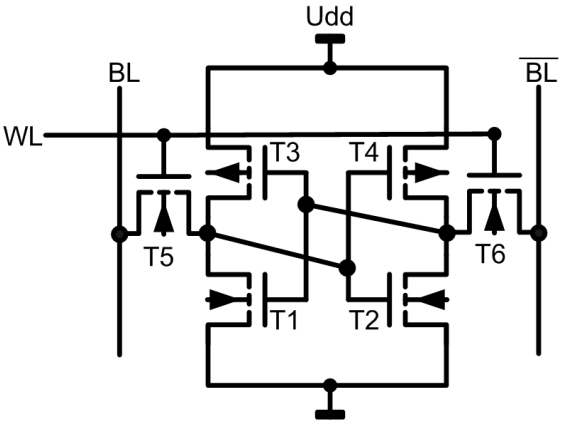

Figure 1 Conventional 6T SRAM cell

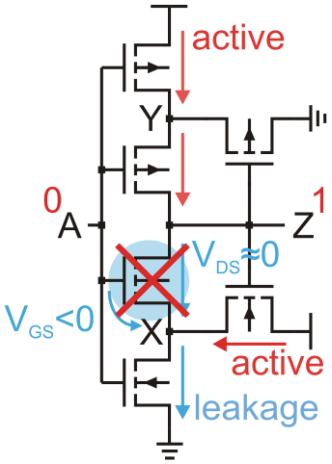

Figure 2 ST-logic based inverter

The conventional implementation of an SRAM cell is the 6T-cell depicted in Figure 1. One of its characteristics is the static noise margin (SNM), a measure for the maximum error signal at the internal nodes that can be tolerated without losing the stored information. Accordingly, SNM should be high. In contrast, a low SNM is preferred during the write access as the state of the cell is flipped on purpose.
As illustrated in Fig. 2, Schmitt-Trigger Logic makes use of feedback in order to maximize the SNM. However, the feedback may be adapted during the write access whereby the aforementioned conflicting requirements on SNM may be met. The research goal of this thesis is thus to evaluate whether Schmitt-Trigger Logic can be applied to the design of SRAM in order to develop a novel architecture, which is capable of retaining the stored data at extremely low voltage levels.

What we expect:
Interests in electronic circuits and their implementation, willingness to familiarize with the topic and the needed simulation equipment, well documented work, and teamwork.

What we offer:
Intensive supervision of the thesis, nice work environment and teamwork, latest simulation software tools, data analysis tools and free space for own ideas.

Starting Date: As soon as possible

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