Diplom/Master Thesis

Design of 2.4GHz Wakeup Receiver for Wireless Sensor Networks

Recently, wireless sensor network (WSN) is getting more attention due to the emerging applications to next generation healthcare. Low power implementation of WSN nodes presents a considerable design challenge, and the transceiver of a WSN node accounts for a majority of the power consumption, so the transceiver should be heavily duty-cycled in order to reduce the power consumption.

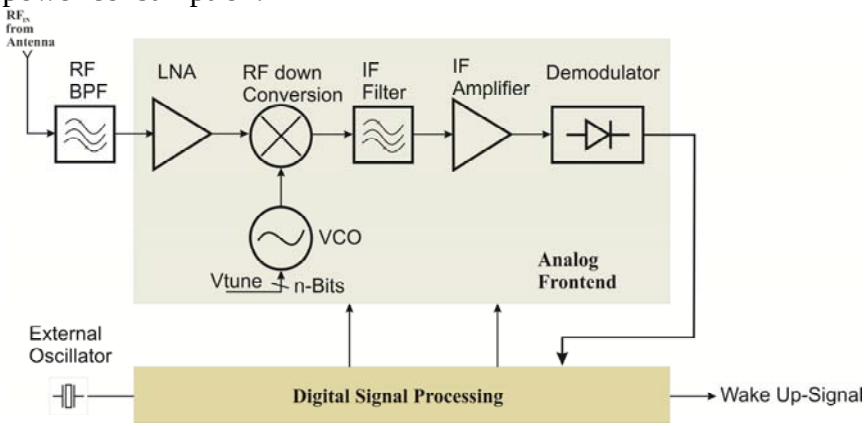

Figure 1: Block diagram of the wakeup receiver including LNA, mixer stage, LC-tuned oscillator, and demodulator.

One key component on a WSN node is the usage of the wake-up receiver, for the efficient duty-cycled communication. The wake-up receiver continuously monitors the channel for requests and activates the transceiver. However, the wake-up receiver should dissipate negligible power compared to the main transceiver, because it is always turned on.

This work will focus on the design and implementation of an ultra-low power wake-up receiver for 400MHz-MICS applications that employs improvement in an amplitude-shift keying. Fig.1 shows the overall architecture of the wake-up receiver. It consists of an RF front-end amplifier and mixing stage, an envelope detector, one baseband amplifier, as well as on-off keying modulation together with a simply RF envelope detector demodulation technique will be considered.

What we expect:
Interests in RF CMOS analog circuit design, knowledge in simulation tools (such as MathLab, Cadence, etc.). Furthermore, well documented work and teamwork.

What we offer:
Intensive supervision of the thesis, nice work environment in a teamwork, latest Simulations-Software tools and measurement instruments, and frees space for own ideas.

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